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EXAMINER
TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/697,364	Applicant(s) BOTALA ET AL.	
	Examiner Joseph D. Torres	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *7-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claims 7-12 are objected to because of the following informalities: "the" is repeated in line 10 of claim 7. Appropriate correction is required.

Claims 8-12 depend from claim 7, hence inherit the deficiencies of claim 7.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the **tester** system" in line 3. There is insufficient antecedent basis for this limitation in the claim. The Examiner assumes the Applicant intended the following in line 3 of claim 1: the test system.

Claims 2-6 depend from claim 1, hence inherit the deficiencies of claim 1.

Claim 7 cites similar language as in claim 1.

Claims 8-12 depend from claim 7, hence inherit the deficiencies of claim 7.

Claim 13 cites similar language as in claim 1.

Claims 14-18 depend from claim 13, hence inherit the deficiencies of claim 13.

Claim 7 recites the limitation "the test program" in line 9. There is insufficient antecedent basis for this limitation in the claim. The Examiner asserts that neither "the test program generator" in line 7 nor the "multi-DUT test program" in line 9 provide antecedent basis for "the test program" nor is it clear what "the test program" in line 9 refers to. The Examiner assumes that the Applicant intended the following: a test program.

Claim 7 recites the limitation "the multi-DUT pattern data" in line 11. There is insufficient antecedent basis for this limitation in the claim. The Examiner assumes that the Applicant intended the following: the multi-DUT pattern data storage area"

Claims 8-12 depend from claim 7, hence inherit the deficiencies of claim 7.

Claim 3 and 15 cites, "the multi-DUT test program makes a plurality of DUTs appear as a single DUT". The Examiner would like to point out that the Applicant fails to explicitly state what aspect or feature of the multi-DUT test program (Note: a DUT has a multitude of features) makes DUTs appear as a single DUT, which renders the claim indefinite. The Examiner assumes the Applicant intended the following in claims 3 and 15: the multi-DUT test program makes a plurality of DUTs appear as a single DUT **by grouping I/O pins of various DUT modules** [Emphasis Added].

Claim 10 cites similar language, i.e., "the multi-DUT pattern data appears to the tester as a pattern data from a single DUT". The Examiner assumes the Applicant intended the following in claim 10: the multi-DUT pattern data appears to the tester **grouped**

together according to pin assignment as **if it were** a pattern data from a single DUT [Emphasis Added].

3. Claims 5, 6, 11 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5 and 17 cite, "the mapping of the plurality of DUTs to the tester system pins occurs independently of restrictions imposed by the test system". "Restriction" is defined in Webster's dictionary as something that restricts. The Examiner asserts that there are a multitude of restrictions on any circuit such a voltage levels, current levels, etc., hence claims 5 and 17 fail to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner assumes the Applicant intended the following in claims 5 and 17: the mapping of the plurality of DUTs to the tester system pins occurs independently of restrictions imposed by having a test system **with multi-DUT tester hardware provided for DUTs of different functional capabilities** [Emphasis Added].

Claim 6 depends from claim 5, hence inherits the deficiencies of claim5.

Claim 11 cites similar language, i.e., "pin data in the pin data storage area is mapped in a manner that would violate tester pin restrictions". The Examiner assumes the Applicant intended the following in claim 10: pin data in the pin data storage area is mapped in a manner that would violate tester pin restrictions **by grouping pins in**

blocks that include pins from DUTs having diff rent functional capabilities

[Emphasis Added].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugamori, Shigeru (US 6331770 B1).

35 U.S.C. 103(a) rejection of claim 1.

Sugamori teaches a method for automatically generating a test environment for testing a plurality of DUTs in a test system (in the Abstract, Sugamori teaches a test system to accommodate a combination of two or more tester modules, i.e., two or more DUTS, and a test fixture provided for electrically connecting tester modules and DUTs, which is

used for automatically generating a test environment for two or more DUTS, Note: in col.6, lines 4-23 and Figure 4, Sugamori teaches that pins operate independently of each other depending on the test purpose under the instruction of event testers 66_1-66_{32}, hence the tester in Sugamori is designed to be able to automatically generate a test environment for multiple DUTs), comprising the steps of: mapping the plurality of DUTs into pins of the tester system (in col. 8, lines 12-22, Sugamori teaches that a host computer is used to control the automatic generation of a test environment by mapping event testers 66_1-66_{32} to I/O pins); inputting into a test program generator pattern data (In col. 6, lines 38-41 and Figure 4, Sugamori teaches that each event tester produces a separate test pattern for each pin from inputted event based information), generic test program rules (col. 4, lines 40-46, Sugamori teaches, for producing a test pattern by using the event based method, it is only necessary to read set/reset data and associated timing data stored in an event memory; read set/reset data and associated timing data are generic test program rules) and the pin data (in col. 8, line 12-22, Sugamori teaches interface 53 is used for transferring pin data from the tester controller 41 to a register in the event tester board to assign the event tester to the input/output pins of the device under test); generating a multi-DUT test program and multi-DUT pattern data; and controlling the test system through the test program (in col. 8, lines 37-39, Sugamori teaches that a multi-DUT test program, transferred from CPU 67 in Figure 5, with event timing information used in developing the multi-DUT pattern data and controlling the operations in the event tester board is stored in Event Memory 60 of Figure 5).

However Sugamori, does not explicitly teach a specific step for creating pin data. The Examiner asserts that, in col. 8, line 12-22, Sugamori teaches interface 53 is used for transferring pin data from the tester controller 41 to a register in the event tester board to assign the event tester to the input/output pins of the device under test, hence the tester in the Sugamori patent requires pin data to make the test equipment in the Sugamori patent operational. In the Summary of columns 4 and 5, Sugamori teaches that the benefit and motivation for using the tester in the Sugamori patent is that it allows for testing of modules having different functional capabilities by providing independent control over pin assignment and pattern generation for the independently assigned pins, hence; one of ordinary skill in the art at the time the invention was made, interested in using the tester to gain the benefits of the tester in the Sugamori patent, would have been highly motivated to create pin data in order to make the test system in the Sugamori patent operational since the tester in the Sugamori patent requires pin data for operation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sugamori by including an additional step of creating pin data. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that creating pin data would provide the opportunity to make the test system in the Sugamori patent operational to gain the benefits of the tester in the Sugamori patent such as independent control over pin assignment and pattern generation for the independently assigned pins (see Summary in col. 4 and 5 of Sugamori).

35 U.S.C. 103(a) rejection of claim 2.

Failure Memory Logic 57 of a single event tester is used for storing fail data from Driver Comparator 61 in Sugamori, see col. 7, lines 55-67, Sugamori.

35 U.S.C. 103(a) rejection of claim 3.

In col. 5, lines 61-67, Sugamori teaches that different devices or different blocks in the device can be tested by a group of test pins, hence Sugamori teaches that the multi-DUT test program makes a plurality of DUTs appear as a single DUT **by grouping I/O pins of various DUT modules** [Emphasis Added].

35 U.S.C. 103(a) rejection of claim 4.

In col. 6, lines 14-20, Sugamori teaches the use of software for controlling event tester modules and in col. 4, lines 40-45, Sugamori teaches independent control of the event testers for each pin.

35 U.S.C. 103(a) rejection of claim 5.

Col. 4, lines 60-65 and col.4, lines 42-46 of Sugamori teach the mapping of the plurality of DUTs to the tester system pins occurs independently of restrictions imposed by having a test system **with multi-DUT tester hardware provided for DUTs of different functional capabilities** [Emphasis Added].

35 U.S.C. 103(a) rejection of claim 6.

Col. 9, lines 50-52 of Sugamori, teach a standardized test fixture and tester modules for use in the step for interfacing, based on the step for pin assignment, as pointed out above, in the rejection to claim 1.

35 U.S.C. 103(a) rejection of claim 7.

Sugamori teaches a pin data storage area which contains pin data which maps the plurality of DUTs into pins of the tester system (in col. 8, lines 12-22, Sugamori teaches that a host computer is used to control the automatic generation of a test environment by mapping event testers 66_1-66_{32} to I/O pins, hence the host computer provides storage for the pin data); a pattern data storage area (Event Memory 58 stores pattern data used in generating event based patterns, see col. 4, lines 40-46), a generic program rules storage area; a test program generator which takes as input the pin data, pattern data and generic program rules (col. 4, lines 40-46, Sugamori teaches, for producing a test pattern by using the event based method, it is only necessary to read set/reset data and associated timing data stored in an event memory; read set/reset data and associated timing data are generic test program rules); a multi-DUT test program which is generated by the test program; a multi-DUT pattern data storage area generated by the test program (in col. 8, lines 37-39, Sugamori teaches that a multi-DUT test program, transferred from CPU 67 in Figure 5, with event timing information used in developing the multi-DUT pattern data and controlling the operations in the event tester board is generated and stored in Event Memory 60 of Figure 5); a tester

containing a plurality of DUTs that has an input from the multi-DUT pattern data and is controlled by the multi-DUT test program (Figure 7A in Sugamori is a diagram of a tester containing a plurality of DUTs that has an input from the multi-DUT pattern data and is controlled by the multi-DUT test program depicted in Figure 4 of Sugamori).

35 U.S.C. 103(a) rejection of claim 8.

Failure Memory Logic 57 of a single event tester is used for storing fail data from Driver Comparator 61 in Sugamori, see col. 7, lines 55-67, Sugamori.

35 U.S.C. 103(a) rejection of claim 9.

In the Summary of columns 4 and 5, Sugamori teaches that the tester in the Sugamori patent allows for testing of modules having different functional capabilities by providing independent control over pin assignment and pattern generation for the independently assigned pins which would include using a single I/O pin for a serial scan test or using a multitude of pins for parallel testing of combinational circuitry.

35 U.S.C. 103(a) rejection of claim 10

In col. 5, lines 61-67, Sugamori teaches that different devices or different blocks in the device can be tested by a group of test pins, hence Sugamori teaches that the multi-DUT pattern data appears to the tester **grouped together according to pin assignment** as **if it were** a pattern data from a single DUT [Emphasis Added].

35 U.S.C. 103(a) rejection of claim 11.

Col. 4, lines 60-65 and col.4, lines 42-46 of Sugamori teach pin data in the pin data is mapped in a manner that would violate tester pin restrictions **by grouping pins in blocks that include pins form DUTs having different functional capabilities** [Emphasis Added].

35 U.S.C. 103(a) rejection of claim 12.

Col. 9, lines 50-52 of Sugamori, teach a standardized test fixture and tester modules for use in the step for interfacing based on the step for pin assignment, as pointed out above, in the rejection to claim 1.

35 U.S.C. 103(a) rejection of claim 13.

Claim 13 substantially cites the same limitations as in claims 1 and 4 providing a means for tangibly embodying a program of instructions for carrying out the method of claims 1 and 4. Host computer 41 in Figure 10 of Sugamori is a means for tangibly embodying a program of instructions for carrying out the method of claims 1 and 4.

35 U.S.C. 103(a) rejection of claim 14.

Failure Memory Logic 57 of a single event tester is used for storing fail data from Driver Comparator 61 in Sugamori, see col. 7, lines 55-67, Sugamori.

35 U.S.C. 103(a) rejection of claim 15.

In col. 5, lines 61-67, Sugamori teaches that different devices or different blocks in the device can be tested by a group of test pins, hence Sugamori teaches that the multi-DUT test program makes a plurality of DUTs appear as a single DUT **by grouping I/O pins of various DUT modules** [Emphasis Added].

35 U.S.C. 103(a) rejection of claim 16.

In col. 6, lines 14-20, Sugamori teaches the use of software for controlling event tester modules and in col. 4, lines 40-45, Sugamori teaches independent control of the event testers for each pin.

35 U.S.C. 103(a) rejection of claim 17.

Col. 4, lines 60-65 and col.4, lines 42-46 of Sugamori teach the mapping of the plurality of DUTs to the tester system pins occurs independently of restrictions imposed by having a test system **with multi-DUT tester hardware provided for DUTs of different functional capabilities** [Emphasis Added].

35 U.S.C. 103(a) rejection of claim 18.

In the Summary of columns 4 and 5, Sugamori teaches that the tester in the Sugamori patent allows for testing of modules having different functional capabilities by providing independent control over pin assignment and pattern generation for the independently assigned pins which would include using a single I/O pin for a serial scan test or using a multitude of pins for parallel testing of combinational circuitry.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Roy, Richard S. et al. (US 6499121 B1) teaches a number of integrated circuit (IC) devices under test (DUTs) having interface circuitry coupled to a single or multi-channel tester for receiving data values from the tester. Kanai, Junichi (US 5216673 A) teaches a plurality of memory devices under test mounted on a test head, the output from each memory device is subjected to a logical comparison with an expected value for each pin and the result of logical comparison is stored in a fail memory. Akar, Armagan A. et al. (US 5216361 A) teaches a plurality of test modules and a receiver for use with a variety of fixture. Matsushita, Shigeru (US 6366109 B1) teaches a semiconductor device with a plurality of pins by applying a test signal includes a tester controller, a logical pin number of a logical pin, pin assignment data, a pin assignment converter, and a test unit. Mydill, Marc R. et al. (US 5025205 A) teaches a test system with reconfigurable architecture. Kuen-Jong Lee, Jih-Jeen Chen and Cheng-Hua Huang; Broadcasting test patterns to multiple circuits, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume: 18 Issue: 12, Dec 1999, Page(s): 1793 –1802.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133
April 10, 2003